CLAIMS

- 1. In a data processing system having a first component and a second component, wherein said first component, the improvement comprising:
 - a. A first data bus having a first set of characteristics responsively coupled between said first component and said second component;
 - b. A second data base having a second set of characteristics responsively coupled between said first component and said second component; and
 - c. A circuit responsively coupled to said first data bus and said second data bus which combines said first data bus and said second data bus into a logical bus having a third set of characteristics wherein said third set of characteristics is different from either said first set of characteristics and said second set of characteristics.
 - 2. A data processing system according to claim 1 wherein said first set of characteristics includes a first maximum transfer rate, said second set of characteristics includes a second maximum transfer rate, and said third set of characteristics includes a third maximum transfer rate and wherein said third maximum transfer rate is greater than either of said first maximum transfer rate and said second maximum transfer rate.

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- 3. A data processing system according to claim 2 wherein said third maximum transfer rate is the sum of said first maximum transfer rate and said second maximum transfer rate.
- 4. A data processing system according to claim 3 wherein said first maximum transfer rate and said second maximum transfer rate are equal.
- 5. A data processing system according to claim 4 wherein said first maximum transfer rate is equal to 33MHz.
- 6. A data processing system comprising:
- a. A first component;
- b. A second component;
- c. A first data bus responsively coupled between said first component and said second component;
 - d. A second data bus responsively coupled between said first component and said second component; and
 - e. A circuit responsively coupled to said first data bus and said second data bus which combines said first data bus and said second data bus into a logical bus.

- 7. A data processing system according to claim 6 wherein said first data bus
- 2 has a first set of characteristics, said second data bus has a second set of
- 3 characteristics, said logical bus has a third set of characteristics, and said third set of
- 4 characteristics if different from said first set of characteristics and said second set of
- 5 characteristics.
- 8. A data processing system according to claim 7 wherein said first set of
- 2 characteristics includes a first data transfer rate, said second set of characteristics
- includes a second data transfer rate, said third set of characteristics includes a third
- data transfer rate, and said third data transfer rate is greater than either of said first
- 5 data transfer rate and said second data transfer rate.
- 9. A data processing system according to claim 8 wherein said third data
- 2 transfer rate equals the sum of said first data transfer rate and said second data
- з transfer rate.
- 10. A data processing system according to claim 9 wherein said first data
- 2 transfer rate is equal to said second data transfer rate.
- 11. A method of coupling a first component to a second component within a
- 2 data processing system comprising:

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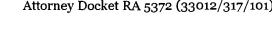
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- a. Providing a first data bus having a first set of characteristics 3 responsively coupled between said first component and said second component; 5
 - b. Providing a second data bus having a second set of characteristics responsively coupled between said first component and said second component; and
 - c. Combining said first data bus and said second data bus to produce a logical bus having a third set of characteristics'
 - 12. A method according to claim 11 wherein said first set of characteristics includes a first data transfer rate, said second set of characteristics includes a second data transfer rate, said third set of characteristics includes a third data transfer rate, and said third data transfer rate is greater than either of said first data transfer rate and said second data transfer rate.
- 13. A method according to claim 12 wherein said third data transfer rate is 1 equal to the sum of said first data transfer rate and said second data transfer rate. 2
- 14. A method according to claim 13 wherein said first data transfer rate is 1 equal to said second data transfer rate. 2

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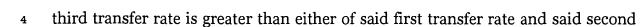
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1	15.	A method	according to	o claim	14	wherein	said	first	data	transfer	rate	is
2	equal to 33	MHz.										

16. An apparatus comprising:

- a. First means for performing a first data processing function;
- b. Second means for performing a second data processing function;
- c. First means responsively coupled to said first performing means and said second performing means for transferring data from said first performing means to said second performing means in accordance with a first set of characteristics;
- d. Second means responsively coupled to said first performing means and said second performing means for transferring data from said first performing means to said second performing means in accordance with a second set of characteristics; and
- e. Means responsively coupled to said first transferring means and said second transferring means for combining said first transferring means and said second transferring means into a logical transferring means having a third set of characteristics.
- 1 17. An apparatus according to claim 16 wherein said first set of characteristics 2 includes a first transfer rate, said second set of characteristics includes a second 3 transfer rate, said third set of characteristics includes a third transfer rate, and said



- 5 transfer rate.
- 18. An apparatus according to claim 17 wherein said third transfer rate equals
- 2 the sum of said first transfer rate and said second transfer rate.
- 1 19. An apparatus according to claim 18 wherein said first transfer rate equals
- 2 said second transfer rate.
- 20. An apparatus according to claim 19 wherein said first transfer rate is equal
- 2 to 33MHz.